SE - SEM III [CBSGS] EXTC 26 May 2015
Digital Electronics

QP Code :4893

(3 Hours) **[Total Marks :80**

N.B. (1) Question no **1** is **compulsory**
(2) Out of **remaining** questions, attempt any **three** questions
(3) **Assume** suitable **data** if required
(4) Figures to the right indicate **full marks**

1.	(a)	Compare combinational logic circuits with sequential circuits	**5**
	(b)	Compare PLA and PAL	**5**
	(c)	Explain static RAM	**5**
	(d)	Explain Master-Slave JK Flipflop	**5**
2.	(a)	State and prove laws of Boolean Algebra	**10**
	(b)	Using Quine McClusky method, minimize the following $F(A, B, C, D) = \sum m(0,2,5,7,8,10,12,15)$	**10**
3.	(a)	Implement Full adder using 8:1 multiplexers	**10**
	(b)	Write VHDL code for 3-bit up counter	**10**
4.	(a)	Design a two bit digital comparator and implement using basic logic gates	**10**
	(b)	Draw a neat circuit of BCD adder using IC 7483	**10**
5.	(a)	What is universal shift register? Explain any two modes of shift register	**10**
	(b)	i) Covert a D FF to T FF	**5**
		ii) Convert a JK FF to T FF	**5**
6.	(a)	Design a Synchronous counter using T FF for the sequence given below: 1-2-3-4-5-6-7-1	**10**
	(b)	Define the following terms for logic families	**10**
		i) Propagation Delay	
		ii) Fan out	
		iii) Power Dissipation	
		iv) Noise Margin	
		v) Fan in	

JP-Con.: 10636-15.